SM Package Miniaturization Trends and Assembly Reliability Challenges

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ABSTRACT

Different aspects of advanced surface mount package technology have been investigated. Three key areas included the assembly reliability of conventional Surface Mount (SM), Ball Grid Arrays (BGAs), and Chip Scale Packages (CSPs). This paper will present the test results as well as lessons learned from design, manufacturing, inspection, and reliability of these assemblies. These findings offer valuable information to designers on package robustness and for better understanding of the challenges associated with the SM technology implementation, particularly new advanced miniaturized CSPs.

KEY WORDS: Solder Joint Reliability, Surface Mount Technology (SMT), Ball Grid Array (BGA), Chip Scale Package (CSP), Thermal Cycling Fatigue

1. MINIATURIZATION TRENDS

SM electronic packages are mounted directly onto surface rather than inserting the leads into plated through-holes (PTHs). There are several surface mount package styles, both active and passive. Active devices are divided into those with terminations of leads on the periphery of the component, two or four sides, or those with terminations (either pads or solder bumps) over much of the bottom of the component. Peripheral array packages (PAP) such as quad flatpack (QFP) have less potential for significant size reduction with increased I/O (input/output) counts compared to area array packages (AAPs). The BGAs from the latter category are now the mainstay alternative to PAPs. For example, the CSP version of the two sided PAP is the lead-on-chip (LOC) package and the versions for AAPs are μBGA™, mini-BGA, and fine pitch BGA packages, generally with eutectic solder balls (see Figure 1).

Another level of miniaturization is accomplished by directly attaching the bare die to the PWB. The direct Flip Chip On Board (FCOB) is the ultimate miniaturization level achieving nearly 70% efficient use of the area of the die ratio to the PWB's footprint. In FCOB, solder bumps are permanently attached to the face of bare die, and the flip side is mounted on the PWB. In Chip-

On-Board, with about 50% use of area efficiency, the pads of the wire bonded die are used for second level wire bonding onto the PWB.

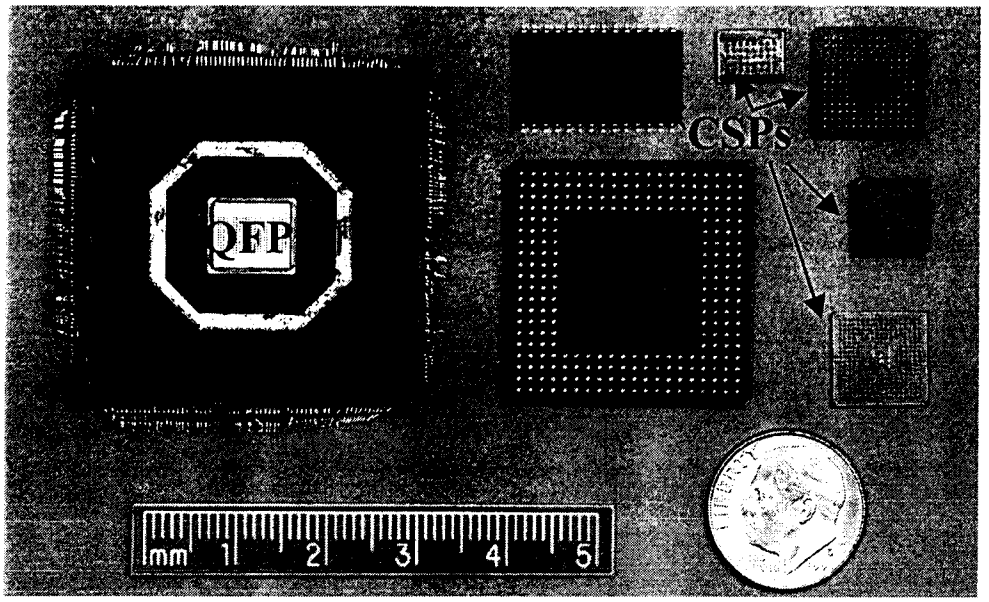

Figure 1 SM miniaturization from QFP to BGA and CSPs

2. ASSEMBLY RELAIBILITY: A SYSTEMS APPROACH

To meet the mission requirements or to bring a product into market successfully, many factors must be considered. Concurrent engineering approaches which consider multifacet areas of technology and interaction among the various engineering disciplines are key in meeting these objectives. The areas that must be included are:

- Design for manufacurability
- Design for testabililty
- Design for quality and reliability.

Figure 2 shows the elements of a successful technology implementation. A similar approach could be used when a subsystem of electronic assemblies is being investigated. The internal JPL teaming arrangement for SMT evaluation (1) as well as the JPL-led industry-wide consortia of BGA (2), MicrotypeBGA (3), and CSP followed the same concurrent engineering approach. This approach is extended here to include various aspects of electronic attachment including manufacturing and design for reliability from conventional SM packages to emerging CSPs.

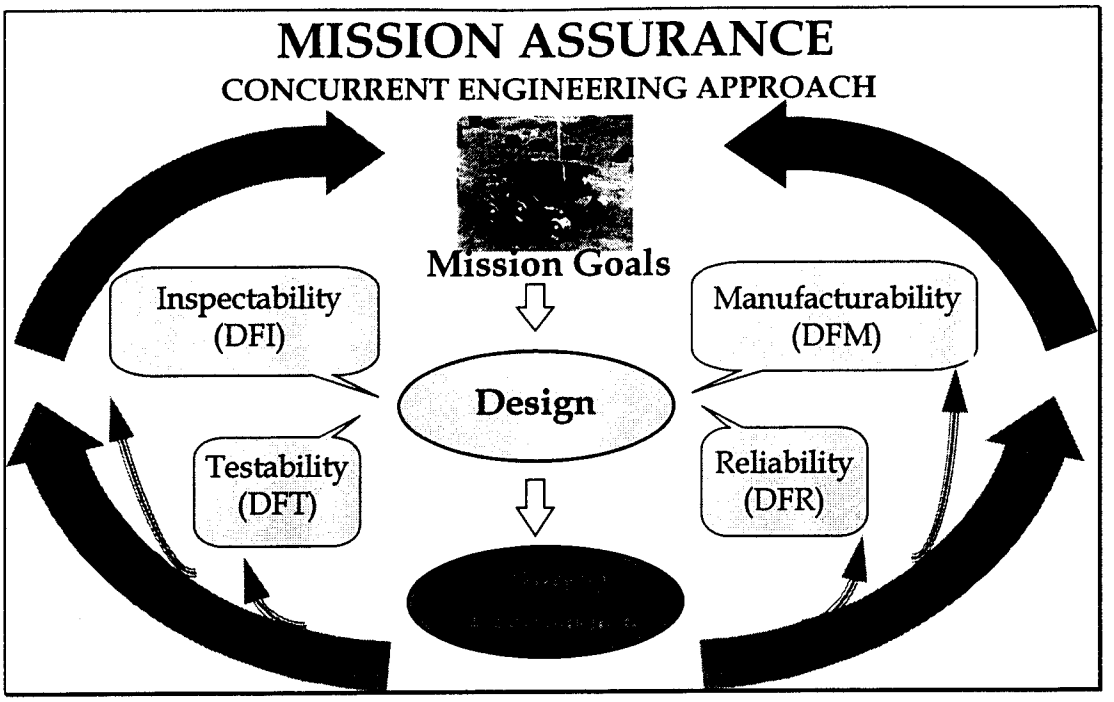

Figure 2 Concurrent Approach for Mission or Product Assurance

3. ATTACHMENT OPTIMIZATION APPROACHES

To communicate input/output signals from package to subsystem of electronic hardware, the package is attached to Printed Wiring Boards (PWB). The attachment is accomplished by various techniques including insertion, plated through hole, surface mount, and adhesive bonding. Only the aspects of attachment by solder will be discussed.

Attachment is generally accomplished by soldering the leads (castellation or endcaps for leadless packages, balls for grid arrays) to the PWB. In surface mount, solder has both electrical and mechanical functions. Thus, for SMT, damage to solder could readily affect functional integrity of the system. Therefore defects that cause changes either in mechanical or electrical system characteristics and their reasons for failure are critical. The most common damage to solder joints are those induced by thermal cycling. The main cause of such damage is considered to be differences in thermal expansion of package and PWB materials. This is especially true for eutectic solder (63Sn/37Pb) which creeps at room temperature. Creep for materials generally occurs at temperatures above half of the absolute melting temperature (T/Tm >0.5). This value is 0.65 at room temperature for eutectic solder. Creep and stress relaxation are main causes of cycling damage.

The main source of damage in package attachment is caused when the system temperatures is changed. Damages to solder joints are most often caused by

- Stress induced by the global CTE (Coefficient of Thermal Expansion) differences between the package and board. The package and board can also have temperature gradients through the thickness and at surface areas
- Local CTE differences between solder attachment to component and PWB

Reducing CTE differences of component and PWB reduces cycling damages, but the ideal condition depends on thermal conditions of components, PWB, and solder. An ideal condition could be selection of PWB materials which have slightly higher CTE than the components. This is based on the assumption that generally the global CTE is dominant and the component is hotter than the PWB.

There are other approaches to reducing damage to solder joints. Underfill application is a common technique which have been widely used for direct attachment of chip on board or when package leads are not robust. Other less conventional approaches are aimed at absorbing CTE mismatch between the die and board internally or externally through strain absorbing mechanisms and therefore reducing stresses on the solder joint interconnect. These approaches could introduce their own unique damage since the weakest link now is transferred from solder joint to other areas of the attachment system.

4. CONVENTIONAL SURFACE MOUNT TECHNOLOGY

The SMT program focused on the use of SMT for high reliability, ultra low volume spacecraft electronics as used in the NASA community. Various aspects of technology were investigated and documented. These include an initial survey, and research on design, modeling, manufacturing, test, and deployment (aging) cycles. Findings from the survey and reliability results for conventional packages are discussed here.

4.1 SMT Survey In a survey, the critical parameters of SMT manufacturing were identified. These included:

- Coplanarity is extremely critical for leaded packages.
- The assembly defects most reported by the QA SMT survey performed by JPL were: insufficient solder, no solder and poor wetting.
- Dewetting was the single most important feature that an inspector should flag.
- Paste qualification tests, inspection following the paste print, part placement and after solder reflow inspections are critical to assure joint integrity.
- Manufacturing analysis tools such as Design of Experiment (DOE) and Statistical Process Control (SPC) are generally used to track solder defects, defect type and location, Generally there was no formal method of tying these defects back to the manufacturing procedures.

It was concluded that the leading causes of SMT rejects were solderability and solder paste deposition problems.

4.2 SMA (Surface Mount Assembly) Reliability Evaluation The SMA test vehicles involved the use of a single ceramic component, 0.050 inch pitch, soldered to an epoxy-fiberglass FR-4 board. LCCs, J-lead cerquads, and gull wing cerquads were the SMT components. Test vehicles were subjected to a thermal cycle profile with long duration to assure near complete creeping. This long duration cycle started at 25°C with a decrease rate of 2°C per minute to -55°C with an oven dwell setting of 45 minutes. The temperature increased to 100°C at a rate of 2°C per minute with an oven dwell setting of 45 minutes, followed by a decrease in temperature to 25°C. The duration of each cycle was 246 minutes.

4.3 SMA Test Results Figure 3 shows cycles to failure for 68-, 28-, and 20-pin LCC assemblies. The cycles to failure were ranked from low to high and failure distribution percentiles were approximated using median plotting position, $F_i = (i-0.3)/(n+0.4)$. As expected, there was a large spread in cycles to failure because of the common variance that are associated with materials and manufacturing conditions including solder joint volume, quality of joint, and location. The first failure for the 68-pin LCCs was detected at 53 cycles while the last sample failed after 139 with 93 average cycles. 28-pin LCCs failed at much higher cycles in the range of 352 to 908 with 660 average cycles. The 20-pin cycles to failure were in the same range as for those of 28-pins and failed within 573 to 863 averaging 674 cycles.

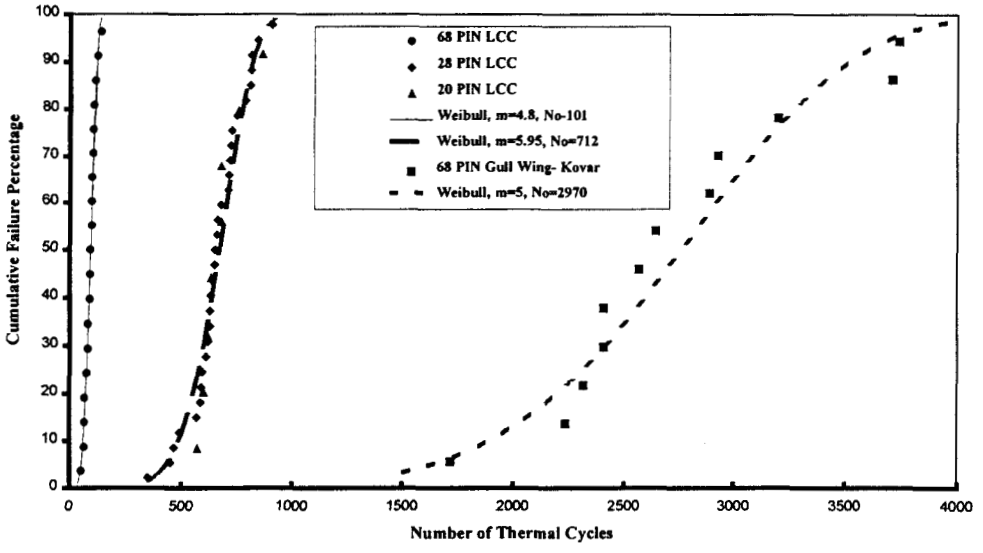

Figure 3 Cumulative Failure Distribution Plots for LCC and Gull Wing Assemblies

If only Distance to Neutral Points (DNPs) are considered, the 20-pin LCCs with shorter DNP than the 28-pin, should have failed at higher cycles since cycles to failure is directly proportional to DNP. However, cycles to failure also inversely depends on the effective solder fillet height. Solder fillet height for 20- and 28-pin LCCs was 0.021 and 0.033 inches respectively, which is lower for a 20-pin resulting in higher shear strain for the same CTE mismatch displacement. The difference in part sizes could have been off-set by the difference in the fillet heights.

All 68-pin gull wing assemblies failed at much higher cycles. Assemblies with Kovar alloy leads were failed between 1,720 cycles and about 3,750 cycles. Cycles to failure are shown in Figure

3. Gull wings with Alloy 42 lead failed at higher cycles and results are not presented here. The testing of the J-leads is still being continued and with no failures to more than 5,000 cycles which includes several hundreds of -55°C to 125°C cycles.

5. BGA TECHNOLOGY

To address many common quality and reliability issues of BGAs, JPL organized a consortium with sixteen members in early 1995. Diverse membership including military, commercial, academia, and infrastructure sectors which permitted a concurrent engineering approach to resolving many challenging technical issues.

BGA is an important technology for utilizing higher pin counts, without the attendant handling and processing problems of the peripheral leaded packages. They are also robust in processing because of their higher pitch (0.050 inch typical), better lead rigidity, and self-alignment characteristics during reflow processing.

BGAs' solder joints cannot be inspected visually and reworked using conventional methods and are not well characterized for multiple double sided assembly processing methods. In high reliability SMT assembly applications, e.g. space and defense, the ability to inspect the solder joints visually has been standard and has been a key factor in providing confidence in solder joint reliability. Inspection techniques such as X-ray can be used to detecting gross manufacturing defects such as solder bridge, but not suitable for detection of other defects such as cracks.

5.1 BGA Test Vehicle Configuration The two test vehicle assembly types were plastic (PBGAs) and ceramic (CBGAs) packages. Both FR-4 and polyimide PWBs with six layers, 0.062 inch thick, were used.

- Plastic packages covered the range from OMPAC (Overmolded Pad Array Carrier) to SuperBGAs (SBGAs). These were:
- Two peripheral SBGAs, 352 and 560 I/O
- Peripheral OMPAC 352 I/O, PBGA 352 and 256 I/O
- Depopulated full array PBGA 313 I/Os
- 256 QFP (Quad Flat Pack), 0.4 mm Pitch

In SBGA, the IC die is directly attached to an oversize copper plate providing better heat dissipation efficiency than standard PBGAs. The solder balls for plastic packages were eutectic (63Sn/37Pb).

Ceramic packages with 625 I/Os and 361 I/Os were also included in our evaluation. Solder balls had high melt temperature composition (90Pb/10Sn) with about 0.035 inch diameters. The high melt balls were attached to the ceramic package with eutectic solder (63Sn/37Pb). At reflow, package side eutectic solder and the PWB side eutectic paste will be reflowed to provide the electro-mechanical interconnects.

Plastic packages had dummy and daisy chains with the daisy chains on the PWB designed to be able to monitor critical solder joint regions. Most packages had four daisy chain patterns, 560 I/O had five, and the QFP had one.

5.2 BGAs- Thermal Cycling Two significantly different thermal cycle profiles were used at two facilities. The cycle A condition ranged -30 to 100°C and had increase/decrease heating rate of 2°C and dwell of about 20 minutes at the high temperature to assure near complete creeping. The duration of each cycle was 82 minutes.

The cycle B condition ranged -55 to 125°C. It could be also considered a thermal shock since it used a three regions chamber: hot, ambient, and cold. Heating and cooling rates were nonlinear and varied between 10 to 15 °C/min. with dwells at extreme temperatures of about 20 minutes. The total cycle lasted approximately 68 minutes. BGA test vehicles were continuously monitored through a LabView system at both facilities.

The criteria for an open solder joint specified in IPC-SM-785, Sect. 6.0, were used as guidelines to interpret electrical interruptions. Generally once the first interruption was observed, there were many additional interruptions within 10% of the cycle life. In several instances, a few non-consecutive early interruptions were not followed by additional interruptions till significantly later stages of cycling. This was found more with plastic packages.

5.3 BGAs- Damage Monitoring Both board and package interface cracking was observed with increasing number of cycles. Figure 4 shows typical failures for the two cycling conditions. Failure under the A conditions were generally from the PWB and for the B conditions were from the package sites. Failure mechanism differences could be explained by global or local stress conditions.

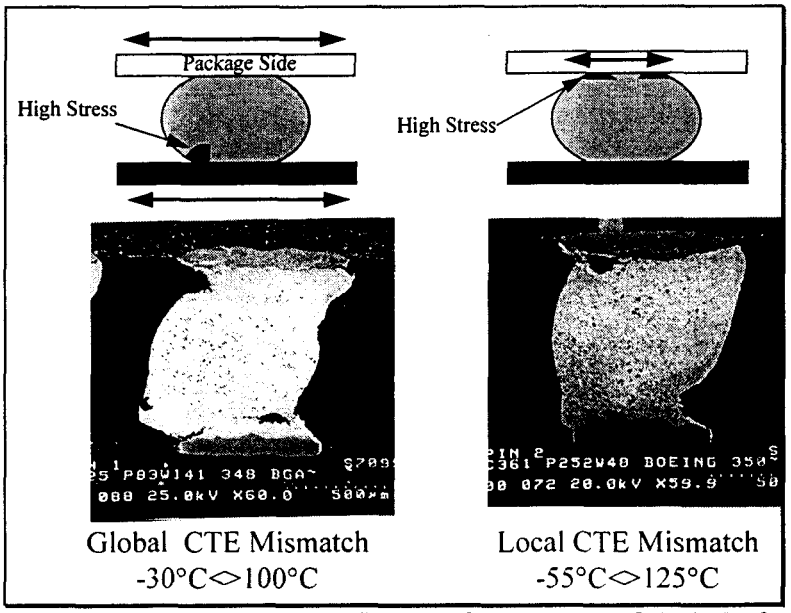

Figure 4 Cross-sections of Failure Sites for CBGA 625 after 350 cycles under A (-30°C to 100°C) and B Conditions

Modeling indicates that the high stress regions shifted from the board to the package themselves when stress conditions changed from the global to local. The A cycling, with slow heat/cooling ramping, allowed the system to reach a uniform temperature, damages could indicate a global stress condition. The B cycle, with rapid heat/cooling, damages could indicate a local stress condition.

Among the plastic packages, the PBGA 313 with depopulated full array balls was first to fail under both B and A thermal cycling conditions. Figure 5 shows various cross- sections of this package's balls from corner to the center at 4,682 A cycles. These photos are for the balls under the die where most damages occur due to local CTE mismatch. Photos with and without voids were also included for comparison. Voids appear to have concentrated at the package interface under the die. Cracking propagation occurred at package or board interfaces for sections with or without voids. The sections with voids were opens indicated by seepage of mounting materials into voids. Except for the interface connecting cracks, there appeared to be no crack propagation among the voids.

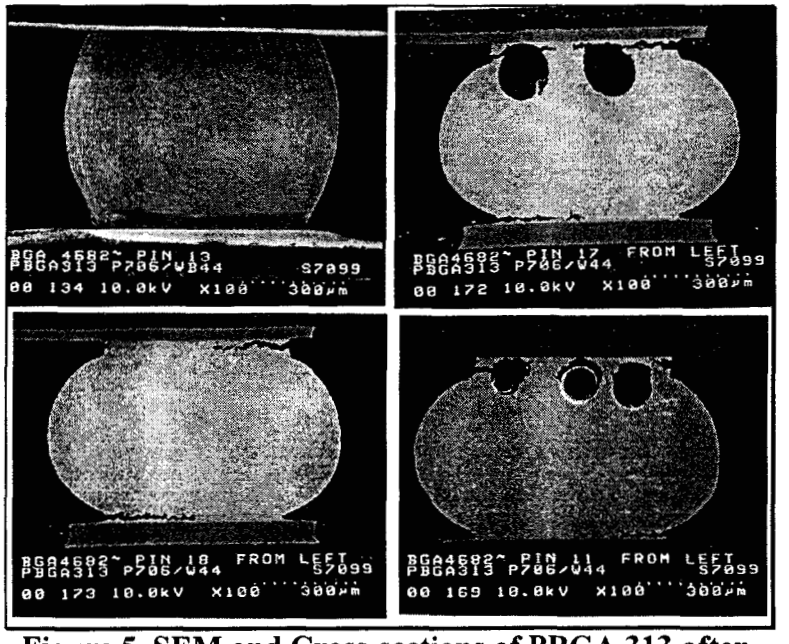

Figure 5 SEM and Cross-sections of PBGA 313 after 4,682 cycles under A (-30°C to 100°C) Conditions

5.4 BGA Thermal Cycling Results Figure 6 shows cycles to first failure for PBGA 313 and SBGA 352 subjected to B cycling for assemblies on polyimide and FR-4 PWBs. The most current PBGA 313 assemblies that failed under cycle A conditions are also included in the plots for comparison. These assemblies include those reflowed with low, standard, and high solder paste levels.

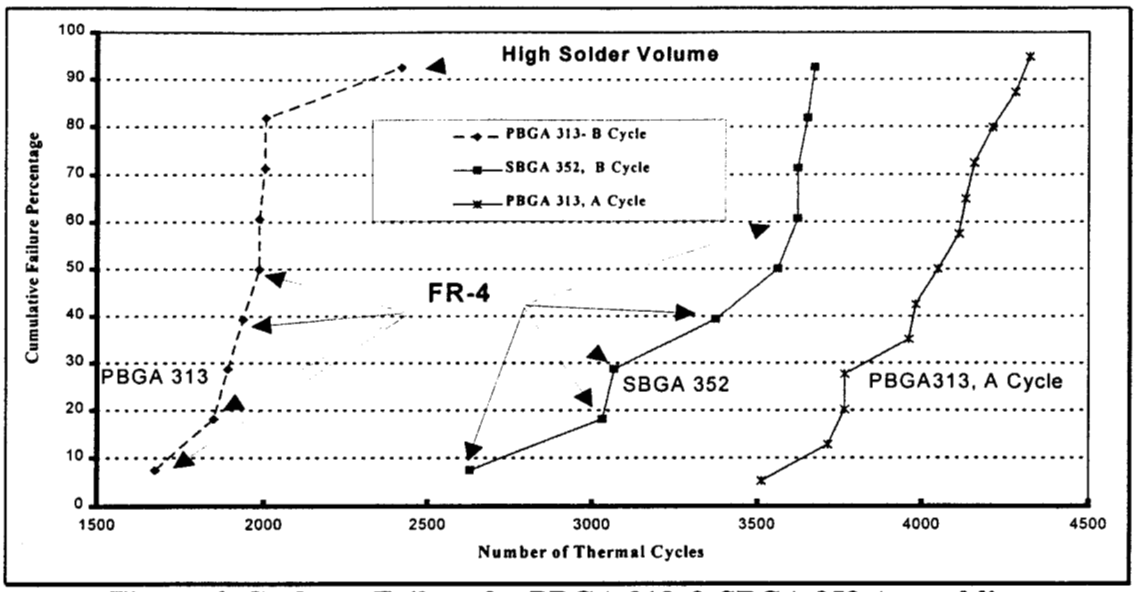

Figure 6 Cycles to Failure for PBGA 313 & SBGA 352 Assemblies (-55°C to 125°C, A) & (-30°C to 100°C)

6. CHIP SCALE PACKAGES

6.1 Why Chip Scale Packages Emerging Chip Scale Packages (CSPs) are competing with bare die assemblies and in most cases are fine pitch version of BGAs. These packages provide the benefits of small size and performance of the bare die or flip chip, with the advantage of standard die packages. CSPs are defined as packages that are up to 1.2 or 1.5 times larger than the perimeter or the area of the die. Many manufacturers now refer to CSP as the package that is a miniaturized version of the previous generation. Two concepts of CSPs are shown in Figure 7. The concepts presented include: (1) packages with flex or rigid interposer and (2) wafer level molding and assembly redistribution.

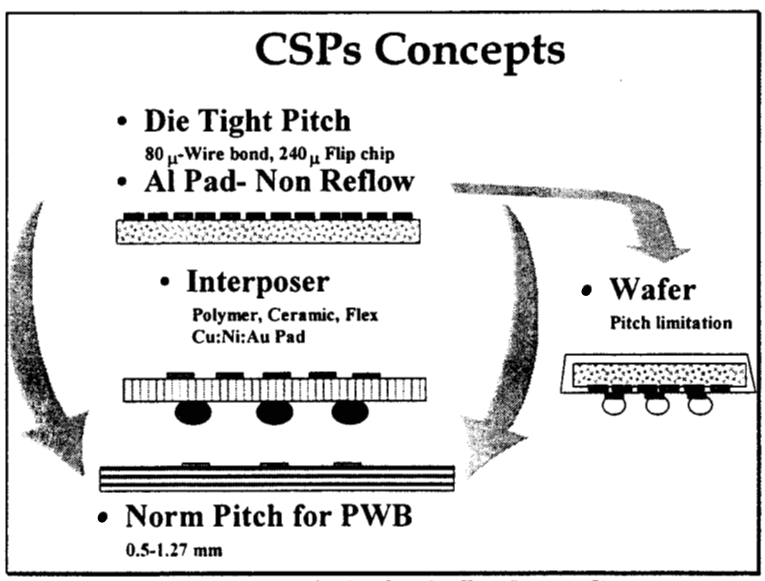

Figure 7 Two Chip Scale Package Concepts

Packaging accomplishes many purposes, including the following:

- Provides solder balls and leads that are compatible with the PWB pad metallurgy for reflow assembly processes.
- Redistributes the tight pitch of the die to the pitch level that is within the norm of PWB fabrication. The small sizes of CSPs do not permit significant redistribution and the current cost effective PWB fabrication limits full adoption of the technology, especially for high I/O counts.
- Protects the die from physical and alpha radiation damages, and provides a vehicle for thermal dissipation.
- Eases die functionality testing.

6.2 Self Alignment of Grid CSPs CSPs can be categorized into grid arrays and leads (no leads) using I/O expandability and manufacturing robustness as shown in Figure 8. Key advantages/disadvantages of each category are also listed. The mini (fine pitch) grid arrays can accommodate higher pin counts, and similarly to BGAs, they have self alignment (centering) characteristics. For BGAs, the ease of package placement requirements has been widely published as one of their attributes. This attribute has permitted reduction in the number of solder joint defects to lower levels than conventional SM packages. Grid CSPs show self alignment, but there is disagreement on what are the best offset limits.

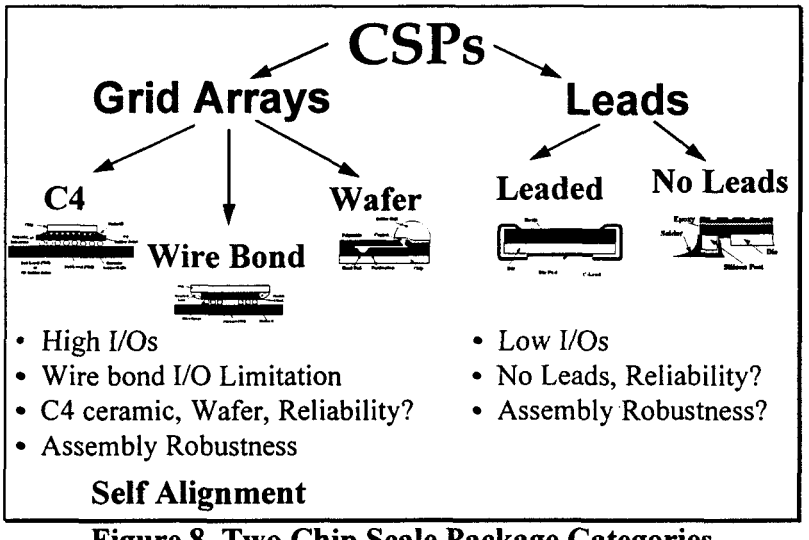

Figure 8 Two Chip Scale Package Categories

7. LESSONS LEARNED AND RECOMMENDATIONS

7.1 Conventional SMT

- CTE differences between the package and board is the key factor affecting solder joint failure by thermal cycling. Creep and stress relaxation are main causes of cycling damages.

- Package size and CTE as well as its CTE absorption capability (e.g., leaded springiness vs no lead) are key factors that define solder joint reliability.
- The leadless ceramic packages with 68 terminations showed lowest cycles to failure followed by 28 and 20 terminations.
- Both 68-pin QFPs and J-leads showed an order of magnitude higher number of cycles to failure than the leadless packages.

7.2 BGA Packages and Assembly Reliability

- BGAs were robust in assembly compared to the 256 fine pitch, 0.4 mm QFPs. All QFPs showed bridging to some degree and had to be reworked.
- Ceramic BGAs failed much earlier than their plastic counterparts because of their much larger CTE mismatch on FR-4/Polyimide boards.
- Cycles to electrical failure for Ceramic BGAs depended on many parameters including cycling temperature range and package size (I/O).
- Ceramic packages with 625 I/Os were first to show signs of failure among the ceramic (CBGA 625 and CBGA 361) and plastic packages (SBGA 560, SBGA 352, OMPAC 352, and PBGA 256) when cycled to different temperature ranges.
- The PBGAs with 313 I/O, depopulated full arrays, were first among the PBGAs to fail within both cycling ranges.
- The 352 SBGA with no solder balls under the die, showed much higher cycles to failure than the PBGA 313.

7.3 CSP Assembly Reliability

- The board level reliabilities of most CSP packages are comparable or better than LCC with similar I/O counts. These packages, however, are not as robust as leaded packages including gull wing and J-leads.
- BGAs and grid CSPs align themselves during the reflow process and therefore some misalignment is acceptable. Acceptable misalignment depends on package type, size, ball material, and weight of package, etc.

The JPL-led consortia are formed to systematically address many of CSP board reliability issues. Understanding the overall philosophy of testing to meet system requirements as well as detecting new failure mechanisms associated with these miniaturized packages is key to collecting meaningful test results.

8. REFERENCES

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9. ACKNOWLEDGMENTS

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10. BIOGRAPHY

Dr. Reza Ghaffarian has nearly 20 years of industrial and academic experience in mechanical, materials, and manufacturing process engineering. At JPL, Quality Assurance Section, he supports research and development activities in SMT, BGA, and CSP technologies for infusion into NASA's missions. He has authored over 50 technical papers and numerous patentable innovations. He received his M.S. in 1979, Engineering Degree in 1980, and Ph.D. in 1982 in engineering from the University of California at Los Angeles (UCLA).